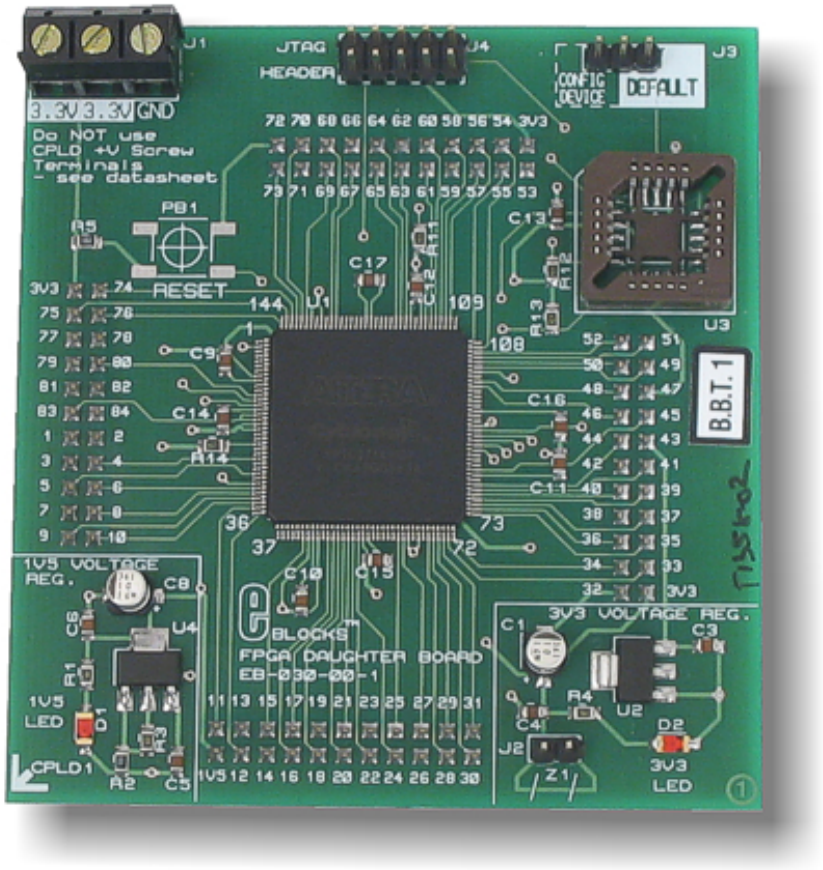
FPGA Board datasheet



Contents

1 About this document

This document concerns the Matrix FPGA Board code EB-030-00-1.

Trademarks and Copyright

Other sources of information

There are various other documents and sources that you may find useful:

Getting started with E-Blocks.pdf

This describes the E-blocks system and how it can be used to develop complete systems for learning electronics.

Disclaimer

The information in this document is correct at the time of going to press. Matrix Multimedia reserves the right to change specifications from time to time.

Technical support

If you have any problems operating this product then please refer to the troubleshooting section of this document first. You will find the latest software updates, FAQs and other information on our web site: www.matrixmultimedia.co.uk. If you still have problems please email us at: support@matrixmultimedia.co.uk.

2 General information

2.1 Description

This FPGA daughter board sits on top of the existing E-blocks CPLD programming board (EB020) to provide 7 full E-blocks ports which can interface to other E-blocks: from simple LED and switch boards through to more complex boards like internet interfaces, IrDA communication systems, internet and Bluetooth boards. The FPGA device used is Altera's EP1C3 FPGA, which contains 3000 Logic Elements. An alternative 6K Logic Element device is also available.

The FPGA is programmed using Altera's Quartus II web edition software and full course notes are available.

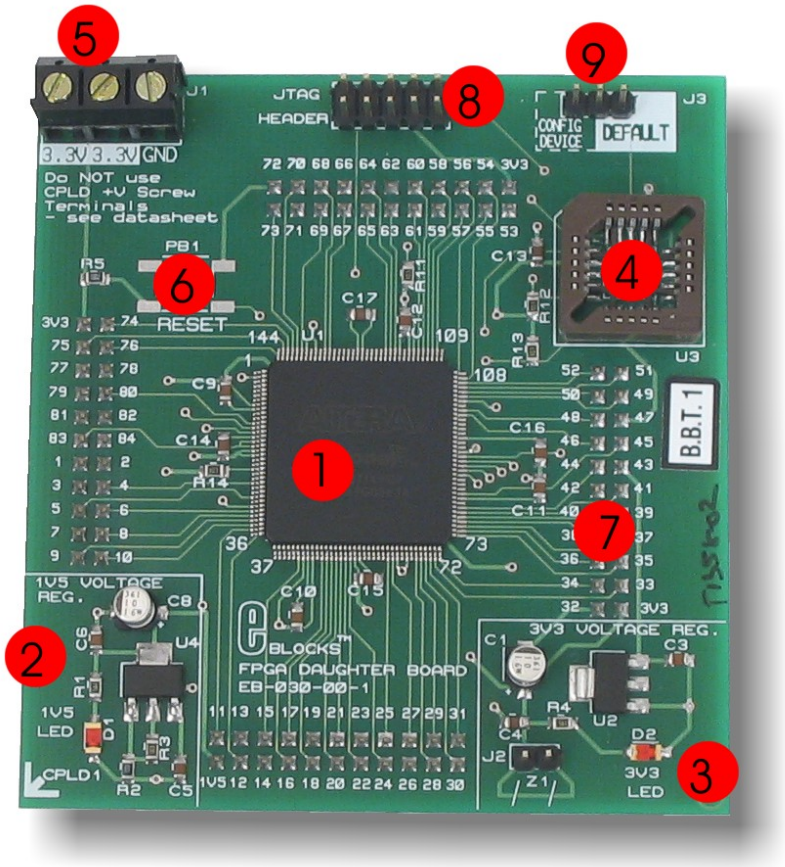
The FPGA daughter board itself can be removed from the CPLD board to provide a leaded component that can be used in your own projects (serial memory programmer required). This solves the difficult issue of handling FPGA packages that are difficult to solder.

Further information on E-blocks is available in a separate document entitled Introduction to E-blocks.doc.

2.2 Features

- E-blocks compatible
- Low cost
- Used as an FPGA development board
- Can be used as a component for further project work
- Full suite of programming software
- 1.5V core voltage and 3.3V I/O voltage – made available via screw terminals
- Socket for reprogrammable configuration (EPC2)
- Programmable 'reset' button
- JTAG interface connector

3 Board overview



1. Altera Cyclone® FPGA
2. 1.5V core voltage regulation circuit
3. 3.3V I/O voltage regulation circuit
4. Configuration device socket
5. Screw terminal (3.3V and GND)
6. Programmable ‘reset’ pushbutton
7. Header sockets – for connection to CPLD board
8. JTAG header extension pins
9. Configuration selection header

4 Getting Started

4.1 Installation instructions - Software

Installing Quartus II
This software a web-based and therefore requires the users to have access to the Internet.

1. Enter the Altera® website at www.altera.com
2. Click 'Design software' under the product header.
3. Now click 'Downloading" under the Ordering & Downloading header.
4. Next, click "Quartus II Web Edition".
5. Follow the on-screen instructions to download the program
   - Please note that this will involve registering to the Altera website.

On completion of the on-screen instructions Quartus II web edition will be fully installed and ready to use.
For the most up-to-date version of this software please visit the Altera web page at: www.altera.com

4.2 Programming the Altera® Cyclone® EP1C3T144C7 or EP1C6T144C7 FPGA

Testing the FPGA Board: flasher-fpga.quartus
The following instructions explain the steps to test and use your FPGA Board. The instructions assume that Quartus II Web Edition is installed and functional. It assumes that the folder "Flasher - FPGA" ("Flasher-FPGA_(6K)" for EP1C6 version) has been copied to a suitable place on your computer.

Follow these instructions to test the FPGA Board (CPLD Board needed)

1) Ensure that the CPLD is removed from the CPLD Board.
2) Insert FPGA Board onto CPLD Board
   - Ensuring that the arrow on the bottom left corner of the FPGA Board points to port CPLD1 on the CPLD Board as this will ensure the correct orientation
3) Insert power is supplied to the CPLD via the power connector (J4 of the CPLD Board)
   - Ensure power switch (SW1) is in the "OFF" position
4) Insert EB-004 LED board into any Port of the CPLD Board
5) Insert Parallel cable from computer into CPLD Board
6) Ensure that the jumper for J3 header pins is in the 'Default' position
7) Turn on the power. Move Switch (SW1) to "ON" position
   - The LED on the CPLD Board (D4) and the Led (D2 3V3 LED) should be illuminated
8) Open Quartus II
9) Open the Flasher-FPGA project
   - File > Open Project
   - Navigate to the Flasher-FPGA folder (Flasher-FPGA_(6K) folder for EP1C6 version) using the pop-up window
   - Double click on "flasher-fpga.quartus"
10) From the Tools menu open up the programmer
    - Tools -> Programmer
11) Click on the following boxes to highlight the programming options
    - Program / Configure

12) Click on “Start Programming” Icon 
    This can found Next to the “HARDWARE” button on the Programming screen
13) This should send the program to the FPGA
    If there is a problem check all cables are connected
14) Check that all the LEDs on the LED board light up
    The sequence is as follows
    i. Each light should light consecutively starting from D0 and ending at D7
    ii. Then the sequence will restart from D0 again
    This should satisfy that the FPGA Board is fully functional!

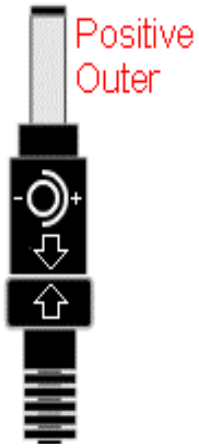
You can reset the program by pressing the “Programmable reset’ button on the FPGA Board.

NOTE Switching SW1 (on the CPLD Board) to the “OFF” position will erase the program in the FPGA – and therefore require it to be reprogrammed.

Ensuring correct polarity for power supply for CPLD Board

Positive Inner/Positive Outer polarity

To set up the correct polarity, the connection symbols on the jack need to match those shown below.



Connector dimensions

The PSU is supplied with a number of connectors. The correct connector for Matrix Multimedia products is:

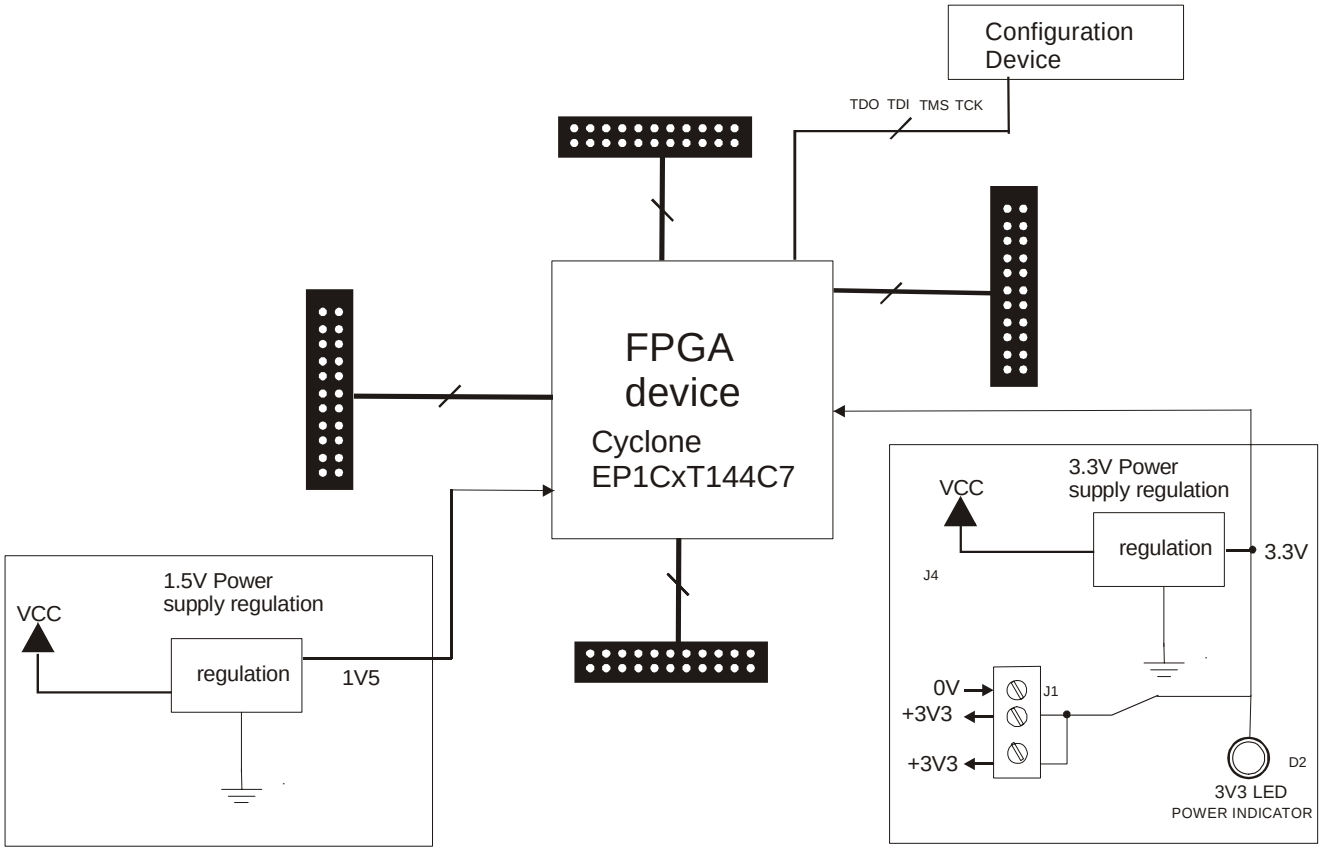
Type D
5.0mm external diameter
2.1mm internal diameter

“**D**” is marked on one side, down by the pins, and “**5.0x2.1**” is marked on the other side.

EB-020-00-1 CPLD Board requires Positive Outer power supply

The two arrows – one on the connector socket and one on the connector pin, help you select the correct side of the power jack, and the symbol shows the correct outer connection.

5 Block schematic and description



The FPGA Board solution is made up of two parts: The FPGA Board and the CPLD Board. The FPGA together with the CPLD board allow the FPGA to be programmed, and the program to be executed 'seamlessly', in the Windows based programming utility Quartus II Web Edition.

5.1 Power Supply

This board requires an input of +5V. This is provided directly from the CPLD Board when the FPGA Board is attached to it – with no extra wiring / configuration needed. The CPLD Board provides the +5V from the header pins. If the board is to be powered externally (not from the CPLD Board) there needs to voltage applied to the header pins (see PIN connections table in the Appendix C for details).

The input voltage is then converted to two different levels: 1.5V and 3.3V. These are generated from LM1117 voltage regulators. The datasheet for these devices can be found at www.national.com/pf/LM/LM1117.html. The 1.5V is the internal core voltage of the FPGA. The 3.3V enables fully tolerant I/O lines for the FPGA. This means that the interface for the FPGA is a 3.3V system. There is an LED (D2) that indicates that the FPGA has received the input voltage and the 3.3V is available to the FPGA. 3.3V is made available from the screw terminal (J1). This can be used to provide other E-Blocks the 3.3V they need.

For information regarding the correct power supply for the CPLD please read the CPLD datasheet EB02030.

Note
Remember that other E-blocks will have to receive +3.3V by placing a connecting wire from the "+3.3" screw terminal of the FPGA to the "+V" screw terminal of each E-Block that requires a voltage. Also note that the FPGA screw terminals should be used and NOT the CPLD board screw terminals. **IMPORTANT Never power "Downstream" E-Blocks using the Vout supply of the CPLD Board.**

5.2 The FPGA

The FPGA that comes with this board is a 144-pin Altera® Cyclone series device. The device has 3000 or 6000 Logic Element – that is approx. 120K or 250K system gates - dependant on the FPGA device on the board. The device has a maximum of 104 I/O lines (note some of them are multiplexed for dual use). This FPGA board utilizes 56 I/O pins, thus providing plenty resources to set up simple or complex projects. On board is also a programmable logic reset pushbutton, connected to a dedicated I/O line. This push button is pulled high via an external resistor, therefore with using this as a program reset, it is an active low reset.

5.3 Crystal operation

The board is NOT fitted with any clocking circuit. The CPLD Board provides a 25MHz clock, automatically routed when the FPGA is inserted in to the CPLD Board.

To make use of the 25MHz crystal, your design must include a "not gate" function between the crystal input (FPGA pin 16, 17, 92 or 93) and the crystal output (FPGA pin 12). The system clock can be taken from the output of the not gate.

The following diagram shows the block schematic, using Quartus, for the necessary circuit to enable the 25MHz crystal. The "clk_in" input is connected to Pin location 93; this is the physical pin for the crystal input. The "clk_out" input is connected to Pin location 12; this is the physical pin for the crystal output. The output of the not gate is used as a system clock to clock all other parts of the circuit.

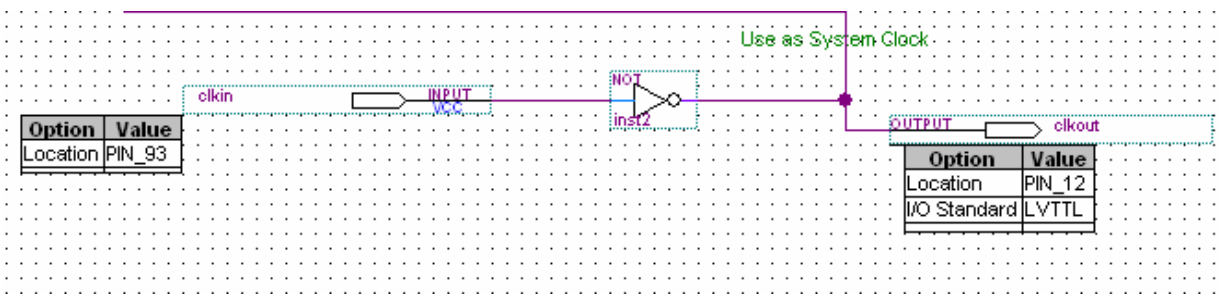


Figure showing the Clock schematic block to enable 25MHz

The following is an example Verilog code to enable the crystal in the design. This design uses the same name as the clock schematic above.

```
/********* Crystal oscillator ***********/
always @ (clk_in)
        begin
                clk_out = !clk_in
        end
/*************************************/
```

An example of VHDL code to use the crystal in your design is shown below. Again this code uses the same names as the above clock schematic.

```
-----------------------------------------------------------------
entity clock_gen is port(
        clk_in: in std_logic;
        clk_out: out std_logic);
end clock_gen;

architecture behave of clock_gen is
begin
        process (clk_in)
                begin
                        clk_out <= not clk_in;
        end process;
end behave;
-----------------------------------------------------------------
```

5.4 DIL Headers and I / O Ports

The FPGA DIL sockets (J12, J13, J14 and J14) are wired to be the exact replica of the CPLD DIL headers. The FPGA Board DIL sockets fit into the CPLD Board DIL headers. The numbers surrounding these 4 DIL header pins shows the appropriate numbers to pins of the CPLD device. Please note that the 4 header blocks have 1 extra input voltage pin, either 3.3V input or 1.5V input – dependant upon the header block – and are marked with either ‘3V3’ or ‘1V5’. These provide a 3.3V or 1.5V input pin when using the FPGA as a component to be used in a separate project.

There are 56 dedicated I/O lines fed out to 7 D-type sockets grouped in ports, each port having 8 I/O lines. The pin-out of these Ports can be found in the Appendix at the end of this document.

WARNING All I/O available are clean signals – this means there is no protection. The user must be aware of this when selecting the functionality of the pins. Avoid connecting +V directly to an I/O pin or two outputs pins directly together – this *can* damage the FPGA device.

5.5 Configuration Device

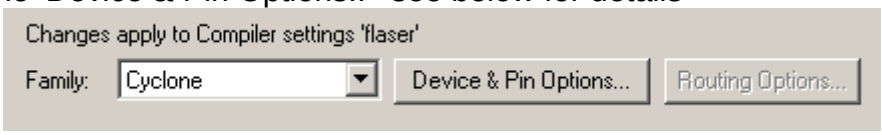
A configuration device is commonly used with FPGAs. The configuration device acts as a memory device for storing the configuration data files for the FPGA. This is particularly useful as FPGAs are not flash based and therefore when the device is powered down, the configuration (or memory) of the device is lost. FPGAs use configuration devices to load the configuration data files when they power up. The FPGA Board has a socket for fitting a configuration device – the EPC2LC20. This configuration is programmed in a 'daisy-chain' effect. The FPGA is programmed then the information is sent to the configuration device. This information sent to the configuration device enables it to control the configuration set-up of the FPGA when powers-up.

The jumper for header pins J3 must be set to "CONFIG DEVICE" on the FPGA board when programming the configuration device.

The Quartus software can automatically generate the configuration data files. The programming of the configuration device is easy. The following steps show the process involved:

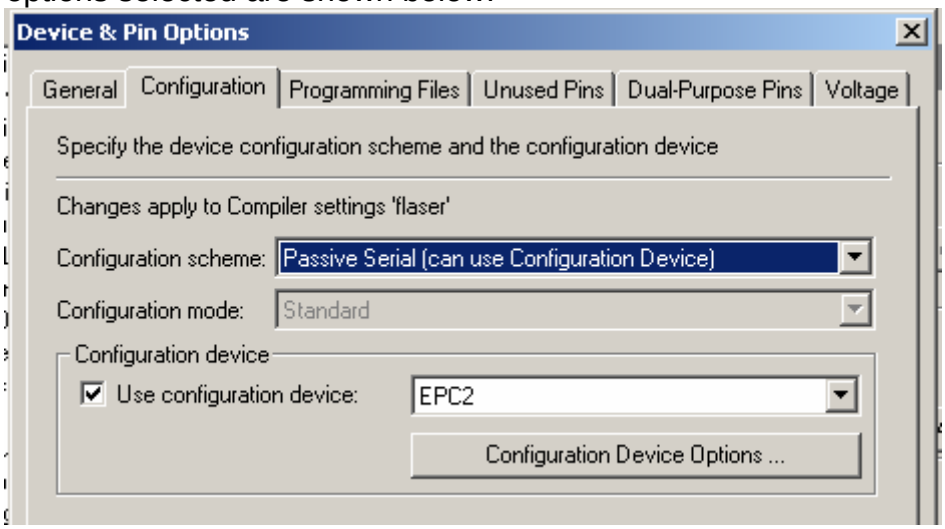
Set-up for use of configuration device
If using a configuration device you must first set-up Quartus to inform it that you want it to compile a configuration device program. This is quite straight forward and once complete will automatically generate a configuration data file.

1. Open the project you want to use.
2. Open the device settings pop-up window
   - Assignment -> Device
3. Click on the 'Device & Pin Options..' see below for details

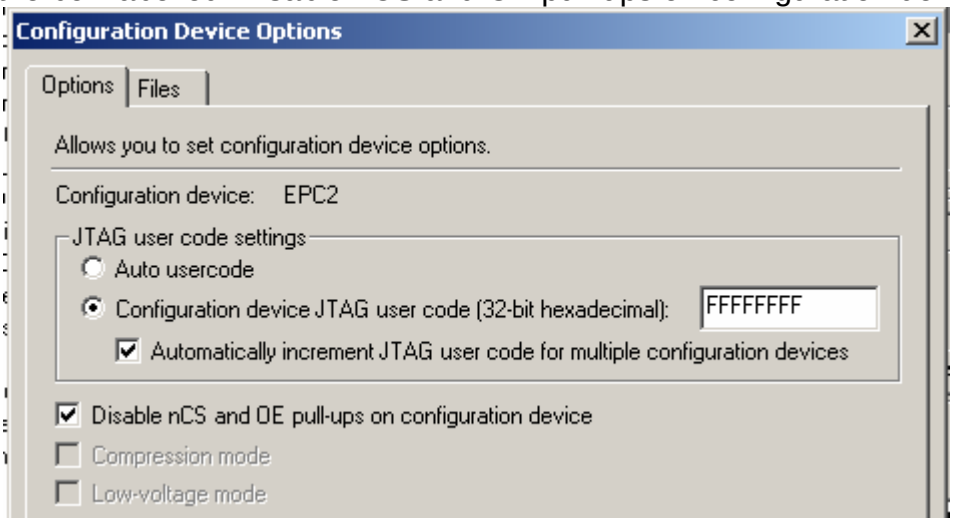


4. In the 'Device & pin options' pop-up window – select the 'Configuration' Tab
5. In this screen select the following options:
   - Configuration scheme: 'Passive Serial (can you configuration device)'
   - Check the box labeled 'Use configuration device'
   - Select 'EPC2' from the drop down window

   The above options selected are shown below.



6. Next press the ‘Configuration Device Options..’ button to get the pop-up window for this option
7. Check the box labelled ‘Disable nCS and OE pull-ups on configuration device’



8. Click ‘OK’ on all the pop-up window screen to save the options and close them down

This is now the software set-up for use with the configuration device.

Now you need to set-up the Hardware. To do this, follow these simple instructions:

1. Ensure that there is no power to the FPGA Board
2. Insert the configuration device – the EPC2LC20 – ensuring correct orientation of the device
3. Set jumper for header pins J3 to ‘CONFIG DEVICE’
4. Enable power to the FPGA Board

This is the hardware set-up for the FPGA configuration device.

The last step is to program the configuration device. This is simple to do now that the software and hardware has been set-up. The following instructions indicate the programming of the configuration device:

1. Recompile the FPGA program (see steps in section “*4.2 Programming the Altera® Cyclone® EP1CxT144C7 FPGA”* for information)
   - Follow the step
   -
2. From the Tools menu open up the programmer
   - Tools -> Programmer

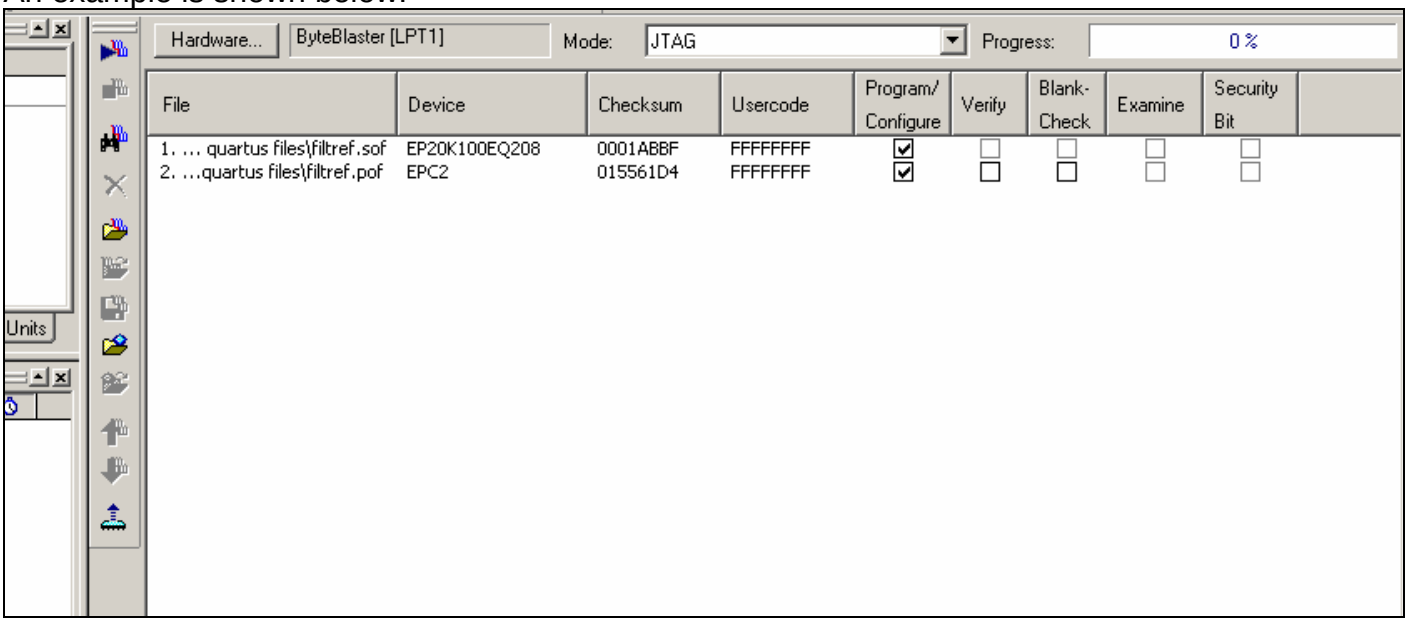
   This should have the FPGA program file in the programmer window, indicated by a file name with and extension .sof (e.g. test_config.sof)
3. Now add the configuration device file (extension .pof)
   - Click on the ‘Open file’ icon in the programmer menu bar (left-hand side of screen)
   - Locate the design folder

- Double click on the file name with the extension .pof (e.g. test_config.pof)

This will have added the configuration device program to the list for programming. The list in the programmer window should include two files:

- .sof extension – FPGA file (also indicated by the device name)
- .pof extension – Configuration device file (also indicated by the device name)

An example is shown below:

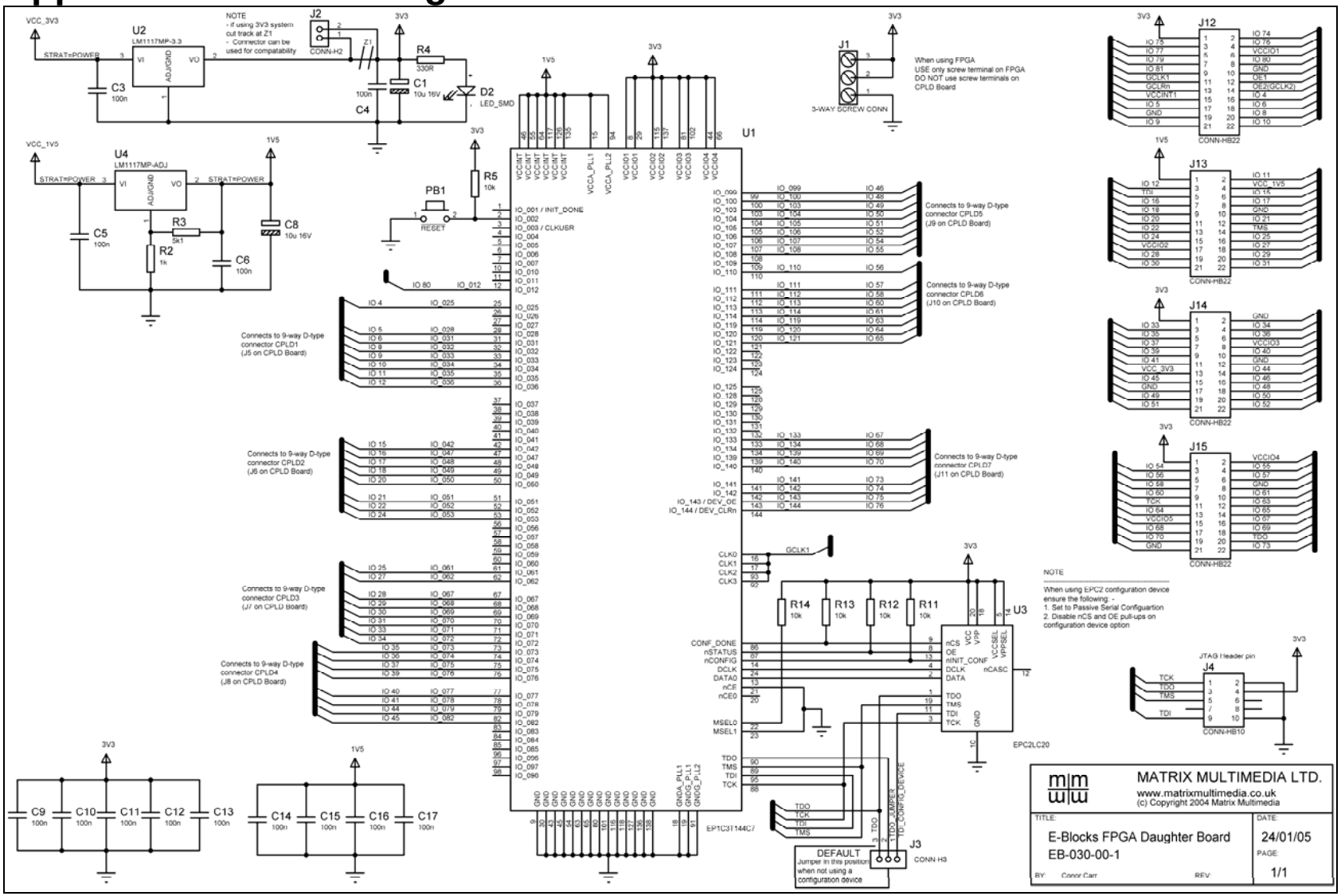


Note the two design files “filtref.sof” and filtref.pof”

4. Click on the following boxes to highlight the programming options for both files (as shown above)
   - Program / Configure
5. Click on “Start Programming” Icon 
   This can found Next to the “HARDWARE” button on the Programming screen
6. This should send the program to the FPGA and to the Configuration device.
7. To test this, remove the power to the FPGA board. This will erase the program from the FPGA. Now when power is reapplied the FPGA should function to that program – as the FPGA loaded the program from the configuration device on power-up.

Note If any error occurs when programming the first thing to check is that the jumper J3 is in the “CONFIG DEVICE” position. If the problem still occurs check the orientation of the configuration device.

Appendix A Circuit Diagram



Appendix B Bus connections

Expansion bus

The following table shows the pin connections on the 9-way D-type ports. This should be used for correctly setting the Pin location in the Quartus software.

Pin Comparison Chart

CPLD1 D-type pin number	FPGA pin number
1	IO 025
2	IO 028
3	IO 031
4	IO 032
5	IO 033
6	IO 034
7	IO 035
8	IO 036
9	GND

CPLD4 D-type pin number	FPGA pin number
1	IO 073
2	IO 074
3	IO 075
4	IO 076
5	IO 077
6	IO 078
7	IO 079
8	IO 082
9	GND

CPLD7 D-type pin number	FPGA pin number
1	IO 133
2	IO 134
3	IO 139
4	IO 140
5	IO 141
6	IO 142
7	IO 143
8	IO 144
9	GND

CPLD2 D-type pin number	FPGA pin number
1	IO 042
2	IO 047
3	IO 048
4	IO 049
5	IO 050
6	IO 051
7	IO 052
8	IO 053
9	GND

CPLD5 D-type pin number	FPGA pin number
1	IO 099
2	IO 100
3	IO 103
4	IO 104
5	IO 105
6	IO 106
7	IO 107
8	IO 108
9	GND

Other important pins

Important Pins	FPGA pin number
Programmable reset	IO 002
Clock input	Pin 16
Clock input	Pin 17
Clock input	Pin 92
Clock input	Pin 93
Clock output	IO 012
TDO	Pin 90
TMS	Pin 89
TDI	Pin 95
TCK	Pin 88

CPLD3 D-type pin number	EPM7128 pin number
1	IO 061
2	IO 062
3	IO 067
4	IO 068
5	IO 069
6	IO 070
7	IO 071
8	IO 072
9	GND

CPLD6 D-type pin number	FPGA pin number
1	IO 110
2	IO 111
3	IO 112
4	IO 113
5	IO 114
6	IO 119
7	IO 120
8	IO 121
9	GND

Appendix C PIN connections

Expansion pin header

The following table shows the pin connections on the 22-way header pins on the FPGA Board.

J12 pin number	Connection		Description
	FPGA Board	CPLD Board	
1	3V3	Not connected	+3.3V
2	IO_142	IO 74	
3	IO_143	IO 75	
4	IO_144	IO 76	
5	Not connected	IO 77	
6	VCCIO	VCC	+5V in
7	Not connected	IO 79	
8	IO_012	IO 80	Osc clock out
9		IO 81	
10		GND	
11	CLK0 CLK1 CLK2 CLK3	GCLK1	Osc clock in
12	Not connected	OE1	
13	Not connected	GCLRn	
14	Not connected	OE2(GCLK2)	
15	Not connected	VCCINT1	
16	IO_025	IO 4	
17	IO_028	IO 5	
18	IO_031	IO 6	
19	GND	GND	
20	IO_032	IO 8	
21	IO_033	IO 9	
22	IO_034	IO 10	

J13 pin number	Connection		Description
	FPGA Board	CPLD Board	
1	1V5	Not connected	+1.5V
2	IO_035	IO 11	
3	IO_036	IO 12	
4	VCC_1V5	VCC	+5V input to 1.5V regulator
5	TDI	TDI	JTAG pin
6	IO_042	IO 15	
7	IO_047	IO 16	
8	IO_048	IO 17	
9	IO_049	IO 18	
10	GND	GND	
11	IO_050	IO 20	
12	IO_051	IO 21	
13	IO_052	IO 22	
14	TMS	TMS	JTAG pin
15	IO_053	IO 24	
16	IO_061	IO 25	
17	Not connected	VCC	
18	IO_062	IO 27	
19	IO_067	IO 28	
20	IO_068	IO 29	
21	IO_069	IO 30	
22	IO_070	IO 31	

J14 pin number	Connection		Description
	FPGA Board	CPLD Board	
1	3V3	Not connected	+3.3V
2	GND	GND	
3	IO_071	IO 33	
4	IO_072	IO 34	
5	IO_073	IO 35	
6	IO_074	IO 36	+5V in
7	IO_075	IO 37	
8	Not connected	VCC	
9	IO_076	IO 39	
10	IO_077	IO 40	
11	IO_078	IO 41	Osc clock in
12	GND	GND	
13	VCC_3V3	VCC	+5V input to 3.3V regulator
14	IO_079	IO 44	
15	IO_082	IO 45	
16	IO_099	IO 46	
17	GND	GND	
18	IO_100	IO 48	
19	IO_103	IO 49	
20	IO_104	IO 50	
21	IO_105	IO 51	
22	IO_106	IO 52	

J14 pin number	Connection		Description
	FPGA Board	CPLD Board	
1	3V3	Not connected	+3.3V
2	Not connected	VCC	
3	IO_107	IO 54	
4	IO_118	IO 55	
5	IO_110	IO 56	
6	IO_111	IO 57	
7	IO_112	IO 58	
8	GND	GND	
9	IO_113	IO 60	
10	IO_114	IO 61	
11	TCK	TCK	JTAG pin
12	IO_119	IO 63	
13	IO_120	IO 64	
14	IO_121	IO 65	
15	Not connected	VCC	
16	IO_133	IO 67	
17	IO_134	IO 68	
18	IO_139	IO 69	
19	IO_140	IO 70	
20	TDO	TDO	JTAG pin
21	GND	GND	
22	IO_141	IO 73	